



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,863	06/01/2001	Steven G. Schmidt	2997.1005-001	1096
21834	7590	04/29/2005	EXAMINER	
BECK AND TYSVER 2900 THOMAS AVENUE SOUTH SUITE 100 MINNEAPOLIS, MN 55416				SHEW, JOHN
ART UNIT		PAPER NUMBER		
				2664

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/872,863	SCHMIDT ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	John L Shew	2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 01/18/2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-58 is/are pending in the application.
- 4a) Of the above claim(s) 47-54 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-2,6,14-17,20,21,23,30-34,44-46 and 55-58 is/are rejected.
- 7) Claim(s) 3-5,7-13,18-19,24-29,35-43 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 October 2001 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>06122002</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Claims 47-54 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected data flow control, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01/18/2005.

### ***Specification***

1. The disclosure is objected to because of the following informalities:

Page 11 line 10 cites "FIG. 5B" should be "FIG. 5A".

Page 16 line 28 cites "logic 448" should be "logic 444".

Page 19 line 2 cites "buffer 434A" should be "buffer 310A".

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 16, 17, 20, 21, 23, 31, 32, 33, 34, 46, 55, 56, 57, 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al.

Claim 1, Yamazaki teaches a method for providing a connection between a source endpoint and a destination endpoint through a fibre channel switch (FIG. 10) referenced by source Termination Node N1 and destination Termination Node N6 through Fabric Switches F1-F3, the method comprising receiving FICON frames at the ingress port of a fibre channel switch from a source endpoint (FIG. 5, column 8 lines 1-31) referenced by Fibre Channel Interface Control Means 10 receiving communication of a frame of a fibre channel, each frame having a header that includes FICON address information (FIG. 11) referenced by Fibre Channel Frame Format including DID address information, mapping the FICON address information of each received FICON frame to internal address information at the ingress port to provide internal frames (FIG. 11, column 11 lines 36-58, column 12 lines 1-7) referenced by the mapping of Fibre Channel Frame Format to addressing of internal ATM cell format, switching the internal frames through the fibre channel switch to an egress port according to the internal address information (FIG. 10, column 12 lines 30-41, column 17 lines 9-31) referenced by the transmission of frame from N1 to N6 through fabrics F1 and F3, and mapping the internal address information of each internal frame to the FICON address information at the egress port for transmission to the destination endpoint (FIG. 7, column 9 lines 36-47, FIG. 18, column 17 lines 32-48) referenced by the Frame Constructing Means generating egress

frames to the destination node with FID to/from Address Header conversion tables used for mapping.

Claim 2, Yamazaki teaches the FICON address information comprises a FICON destination address (FIG. 11) referenced by the destination ID DID of the frame header, and the internal address information includes an internal destination address (FIG. 11) referenced by the Address Header of the ATM Cell, and wherein mapping the FICON address information includes mapping the FICON destination address to an internal destination address (FIG. 14, FIG. 15, column 14 lines 43-58, column 15 lines 1-2) referenced by the Address Header Producing Section using a NID to Address Header mapping table.

Claim 6, Yamazaki teaches the fibre channel switch is one of a plurality of fibre channel switches of a fibre channel switch fabric (FIG. 10) referenced by the switch fabrics F1-F3, and further comprising preassigning a chassis address to the fibre channel switch (column 16 lines 14-25) referenced by the assignment of a NID associated to the switch, each chassis having a specific switch address that is different from the preassigned chassis address (column 16 lines 14-25) referenced by the FID assigned to the switch being different from the NID.

Claim 16, Yamazaki teaches a switch for providing a connection between a source endpoint and a destination endpoint (FIG. 10, column 17 lines 9-31) referenced by

switch Fabric F1 connecting source Termination Node N1 to destination Termination Node N6, the switch comprising an ingress port for receiving inbound FICON frames from a source endpoint (FIG. 8, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre channel frames, each frame having a header that includes FICON address information (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, an address adaptor for mapping the FICON address information of each received FICON frame to internal address information to provide internal frames (FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the Address Header Producing Section 141 using a address header conversion table, and a switch element for switching the internal frames according to the internal address information (FIG. 8) referenced by the ATM Switch Device 160.

Claim 17, Yamazaki teaches the FICON address information comprises a FICON destination address (Fig. 11) referenced by the DID field 610 of the Frame Header, and the internal address information includes an internal destination address (FIG. 11) referenced by the Address Header Producing Means generating an Address Header, and wherein the address adaptor is operable to map the FICON destination address to an internal destination address (FIG. 14, FIG. 15) referenced by the NID to Address Header mapping table.

Claim 20, Yamazaki teaches a second address adaptor for mapping the internal address information of each internal frame to the FICON address information to provide outbound FICON frames (FIG. 8, column 9 lines 36-42) referenced by the Frame Constructing Section 150, and an egress port for transmitting the outbound FICON frames to a destination endpoint (FIG. 8) referenced by the Fibre Channel Interface Control Section 110.

Claim 21, Yamazaki teaches the FICON address information comprises a FICON destination address (Fig. 11) referenced by the DID field 610 of the Frame Header, and the internal address information includes an internal destination address (FIG. 11) referenced by the Address Header Producing Means generating an Address Header, and wherein the second address adaptor is operable to map the internal destination address to a FICON destination address (FIG. 8, column 9 lines 36-42, FIG. 18, column 17 lines 9-48) referenced by the Frame Constructing Section 150 using corresponding conversion tables.

Claim 23, Yamazaki teaches the switch is one of a plurality of fibre channel switches of a fibre channel switch fabric (FIG. 10) referenced by the switch fabrics F1-F3, and wherein a chassis address is preassigned to the fibre channel switch (column 16 lines 14-25) referenced by the assignment of a NID associated to the switch, each chassis having a specific switch address that is different form the preassigned chassis address

(column 16 lines 14-25) referenced by the FID assigned to the switch being different from the NID.

Claim 31, Yamazaki teaches a fibre channel switch (FIG. 9) referenced by switching Fabric F1, an address adaptor (FIG. 8) referenced by the Fibre Channel Port Section 100, comprising an inbound frame processor for receiving inbound frames from a source endpoint (FIG. 8) referenced by the Fibre Channel Interface Control Section 110 receiving input frames, each inbound frame having a header that includes first address information having a first format (FIG. 11) referenced by the Fibre Channel Frame Format including a first address DID field, the inbound frame processor including address logic for mapping the first address information of each received inbound frame (FIG. 14, FIG. 15) referenced by the Address Header Producing Section 141 using NID to Address Header conversion tables, to a second address information having a second format to provide inbound internal frames to a switch fabric (Fig. 11) referenced by the Address Header Producing Means generating the internal ATM Cell address header field, and an outbound frame processor for receiving outbound internal frames from a switch fabric (FIG. 8) referenced by the Frame Constructing Section 150, the outbound frame processor including address logic for mapping the second address information of each outbound internal frame to first address information having the first format to provide outbound frames for transmission to a destination endpoint (FIG. 11, FIG. 18, column 9 lines 36-42) referenced by the construction of a fibre channel frame for transmission to a termination node endpoint.

Claim 32, Yamazaki teaches the first format has continuous addressing (FIG. 11) referenced by the Fibre Channel Frame Format use of the DID field, and the second format has discontinuous addressing (FIG. 17) referenced by the Address Header Producing Means using two separate address header conversion tables for parts of the DID register.

Claim 33, Yamazaki teaches the first format is FICON format (FIG. 11) referenced by the Fibre Channel Frame Format and the second format is an internal format (FIG. 11) referenced by the ATM Cell format.

Claim 34, Yamazaki teaches the FICON address information comprises a FICON destination address (FIG. 11) referenced by the Fibre Channel Frame Format's DID field of the Frame Header, and the internal address information includes an internal destination address (FIG. 11) referenced by the Address Header Producing Means generating the Address Header of the internal ATM cell, and wherein the address adaptor is operable to map between a FICON destination address to an internal destination address (FIG. 15) referenced by the NID to Address Header conversion table.

Claim 46, Yamazaki teaches a switch for providing a connection between a source endpoint and a destination endpoint (FIG. 10, column 17 lines 9-31) referenced by

switch Fabric F1 connecting source Termination Node N1 to destination Termination Node N6, the switch comprising means for receiving FICON frames from a source endpoint (FIG. 8, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre channel frames, each frame having a header that includes a FICON destination address (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, a means for mapping the FICON destination address of each received FICON frame to an internal destination address to provide internal frames (FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the Address Header Producing Section 141 using an address header conversion table, means for switching the internal frames through the switch according to the internal address information (FIG. 8) referenced by the ATM Switch Device 160, means for mapping the internal destination address of each internal frame to the FICON destination address for transmission to the destination endpoint (FIG. 8, column 9 lines 36-42, FIG. 15) referenced by the Frame Constructing Section 150 using conversion tables.

Claim 55, Yamazaki teaches a method for providing a connection between a source endpoint and a destination endpoint through a data switch (FIG. 10, column 17 lines 9-31) referenced by switch Fabric F1 connecting source Termination Node N1 to destination Termination Node N6, the method comprising receiving inbound frames at the ingress port of the data switch from a source endpoint (FIG. 8, FIG. 11, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre

channel frames, each frame having a header that includes a first destination address (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames (FIG. 11, FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the Address Header Producing Section 141 generating an Address Header for the internal ATM cell using an address header conversion table, switching the internal frames through the data switch to an egress port according to the internal address information (FIG. 8, column 17 lines 9-31) referenced by the ATM Switch Device 160 switching data from ingress node N1 to egress node N6, mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint (FIG. 8, column 9 lines 36-42, FIG. 15) referenced by the Frame Constructing Section 150 using conversion tables.

Claim 56, Yamazaki teaches a switch for providing a connection between a source endpoint and a destination endpoint (FIG. 10, column 17 lines 9-31) referenced by switch Fabric F1 connecting source Termination Node N1 to destination Termination Node N6, the switch comprising an ingress port for receiving inbound frames from a source endpoint (FIG. 8, FIG. 11, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre channel frames, each frame having a header that includes a first destination address (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, an address

adaptor for mapping the first destination address information of each received frame to internal address information to provide internal frames (FIG. 11, FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the Address Header Producing Section 141 generating an Address Header for the internal ATM cell using an address header conversion table, a switch element for switching the internal frames according to the internal address information (FIG. 8, column 17 lines 9-31, FIG. 11) referenced by the ATM Switch Device 160 switching data from ingress node N1 to egress node N6 Address Header information of the internal ATM cell.

Claim 57, Yamazaki teaches a method for providing a connection between a source endpoint and a destination endpoint through a network of data switches (FIG. 10, column 17 lines 9-31) referenced by switches Fabric F1-F3 connecting source Termination Node N1 to destination Termination Node N6, the method comprising receiving inbound frames at the ingress port of a first data switch in the network from a source endpoint (FIG. 8, FIG. 11, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre channel frames, each frame having a header that includes first destination address information (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames (FIG. 11, FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the Address Header Producing Section 141 generating an Address Header for the internal ATM cell using an

address header conversion table, switching the internal frames through the network of data switches to an egress port of a second data switch in the network according to the internal destination address information (FIG. 8, FIG. 10, column 17 lines 9-31) referenced by the ATM Switch Devices 160 of Fabrics F1-F3 switching data from ingress node N1 to egress node N6, mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint (FIG. 8, column 9 lines 36-42, FIG. 15) referenced by the Frame Constructing Section 150 using conversion tables.

Claim 58, Yamazaki teaches a network of data switches for providing a connection between a source endpoint and a destination endpoint (FIG. 10, column 17 lines 9-31) referenced by switches Fabric F1-F3 connecting source Termination Node N1 to destination Termination Node N6, at least one ingress port at a first data switch in the network for receiving inbound frames from a source endpoint (FIG. 8, FIG. 11, column 10 lines 11-40) referenced by Fibre Channel Interface Control Section 110 receiving fibre channel frames, each frame having a header that includes first destination address information (FIG. 11) referenced by the Fibre Channel Frame Format including a header with a DID destination ID field, at least one address adaptor at the first data switch for mapping the first destination address information of each received frame to internal address information to provide internal frames (FIG. 11, FIG. 14, column 12 lines 30-41, column 15 lines 3-7) referenced by the switch Fabric F1 Address Header Producing Section 141 generating an Address Header for the internal ATM cell using an address

header conversion table, at least another address adaptor at a second data switch in the network for mapping the internal destination address information of each internal frame to the first destination address information to provide outbound frames (FIG. 8, FIG. 15) referenced by the switch Fabric F3 Frame Constructing Section 150 using conversion tables to construct the fibre channel frame format, at least one egress port at the second data switch for transmitting the outbound frames to a destination point (FIG. 8) referenced by the switch Fabric F3 Fibre Channel Interface Control Section transmitting outbound frames to the termination node N6.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 14, 15, 30, 44, 45, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki as applied to claims 1, 2, 6, 16, 17, 20, 21, 23, 31, 32, 33, 34, 46, 55, 56, 57, 58 above, and further in view of Halsall.

Art Unit: 2664

Claims 14, 15 Yamazaki teaches a fibre channel fabric using fibre channel frame format conversion to an internal ATM Cell format (FIG. 11, Fig. 12) referenced by mapping of fibre channel frame format to ATM Cell. Yamazaki teaches the FICON frame includes a cyclic redundancy check (CRC) (FIG. 11) referenced by the Fibre Channel Frame Format including a CRC field, and wherein mapping the FICON address information to internal address information (FIG. 11) referenced by the Address Header Producing Means mapping the DID to ATM Cell address. Yamazaki teaches the internal ATM Cell Format (FIG. 12) referenced by the standard ATM Cell Format. Yamazaki does not teach the recalculating the CRC for the internal frame, but does show the field HEC in the standard ATM format.

Halsall teaches recalculating the CRC and inserting the recalculated CRC into the internal frame (Fig. 10.7, pp. 577) referenced by the HEC field defined as Header Error Checksum which is a CRC on the first 4 octets of the header which requires recalculating the CRC for the internal standard ATM format.

Halsatll teaches the HEC is a CRC field in the internal address ATM cell.

Yamazaki teaches the mapping the internal address information to FICON address information includes recalculating the CRC and inserting the recalculated CRC into the FICON frame at the egress port (FIG. 11, FIG. 12, column 9 lines 36-42) referenced by the HEC field of the ATM cell which is recalculated to the Fibre Channel Frame Format including the CRC field.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clarify the definition of the HEC field as disclosed by Halsall to the ATM format as disclosed by Yamazaki for the purpose of data checksum verification.

Claim 30, Yamazaki teaches the FICON frame includes a cyclic redundancy check (CRC) (FIG. 11) referenced by the Fibre Channel Frame Format including a CRC field, and wherein mapping the FICON address information to internal address information (FIG. 11) referenced by the Address Header Producing Means mapping the DID to ATM Cell address. Yamazaki teaches the internal ATM Cell Format (FIG. 12) referenced by the standard ATM Cell Format. Yamazaki teaches the address adaptor generates the internal ATM cell (FIG. 8) referenced by the Cell Producing Section 140. Yamazaki does not teach the recalculating the CRC for the internal frame, but does show the field HEC in the standard ATM format.

Halsall teaches recalculating the CRC and inserting the recalculated CRC into the internal frame (Fig. 10.7, pp. 577) referenced by the HEC field defined as Header Error Checksum which is a CRC on the first 4 octets of the header which requires recalculating the CRC for the internal standard ATM format.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clarify the definition of the HEC field as disclosed by Halsall to the ATM format as disclosed by Yamazaki for the purpose of data checksum verification.

Claims 44, 45 Yamazaki teaches a fibre channel fabric using fibre channel frame format conversion to an internal ATM Cell format (FIG. 11, Fig. 12) referenced by mapping of fibre channel frame format to ATM Cell. Yamazaki teaches the inbound frame includes a cyclic redundancy check (CRC) (FIG. 11) referenced by the Fibre Channel Frame Format including a CRC field, and wherein the inbound frame processor is operable mapping the FICON address information to internal address information (FIG. 11) referenced by the Address Header Producing Means mapping the DID to ATM Cell address. Yamazaki teaches the internal ATM Cell Format (FIG. 12) referenced by the standard ATM Cell Format. Yamazaki does not teach the recalculating the CRC for the internal frame, but does show the field HEC in the standard ATM format.

Halsall teaches recalculating the CRC and inserting the recalculated CRC into the internal frame (Fig. 10.7, pp. 577) referenced by the HEC field defined as Header Error Checksum which is a CRC on the first 4 octets of the header which requires recalculating the CRC for the internal standard ATM format.

Halsatll teaches the HEC is a CRC field in the internal address ATM cell. Yamazaki teaches the outbound frame processor is operable to mapping the internal address information to FICON address information thus includes recalculating the CRC and inserting the recalculated CRC into the FICON frame at the egress port (FIG. 11, FIG. 12, column 9 lines 36-42) referenced by the HEC field of the ATM cell which is recalculated to the Fibre Channel Frame Format including the CRC field.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to clarify the definition of the HEC field as disclosed by Halsall to the ATM format as disclosed by Yamazaki for the purpose of data checksum verification.

***Allowable Subject Matter***

4. Claims 3-5, 7-13, 18-19, 22, 24-29, 35-36, 37-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Citation of Prior Art***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent 6260079, White discloses a system for enhancing fibre channel loop resiliency. Patent 6298398, Elliott discloses a method to provide checking on data transferred through fibre channel adapter cards.

Art Unit: 2664

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

js



WELLINGTON CHIN  
SUPERVISORY PATENT EXAMINER